

Rees et al. utterly fails to disclose every element of the claimed invention. This rejection under § 102(b) is therefore in error, and must be withdrawn.

Here, the present application includes independent claims 1 and 28, which recite elements not found in Rees et al. Claim 1, for example, defines a system for monitoring the operation of computer programs by collecting software related events. As recited in the claims, the software related events relate to the performance of a respective target program and are received from target programs by a corresponding event collection card. Each collection card is installed on the same system bus as the card's respective target program and includes a time stamp clock to time stamp each event as it is received. A sync control unit synchronizes the time stamp clock to a sync signal received by a sync interface. A collection control unit time stamps the collected events according to the synchronized time stamp clock and stores the time stamped event in an event memory. Each collection card sends the collected software related events to a host computer that monitors the performance of the target programs based on the collected events.

As pointed out in the prior response, however, Rees et al. does not disclose a plurality of event collection cards that receive a synch signal to synchronize a time stamp clock included on the card, as recited in claims 1 and 28. While Rees et al. discloses connecting a probe 20 to a computer bus to receive tags from an instrumented computer program code running on the computer bus, the clock of probe 20 is not synchronized to any received sync signal. In Rees et al., each probe 20 has its own clock used to time stamp the received tags. (See "Probe Tip Clock" of Fig. 7; col. 12, lines 20-24). But absolutely nothing in Rees et al. describes synchronizing respective clocks of a plurality of probes 20 to a received sync signal.

More specifically, Rees et al. does not disclose at least a "sync control unit for synchronizing the time stamp clock to the sync signal received by the sync interface," as recited in claim 1, or "synchronizing a time stamp clock to the received sync signal," as recited in claim 28. In the outstanding Office Action, the Examiner errs in relying on col. 12, lines 10-20 of Rees et al. for a teaching of this element. Again, this portion of Rees et al. simply describes a clock control circuit for synchronizing a tag to the clock (i.e., time stamping the tag). It bears no relevance to synchronizing the clock before time stamping the tag. Thus, it does not disclose, as

recited in claims 1 and 28, synchronizing the clock to a sync signal and then time stamping a received tag or event according to the synchronized clock.

Therefore, for at least these reasons, claims 1 and 28 are allowable over Rees et al., and the rejection under § 102(b), therefore, must be withdrawn. If, however, the Examiner continues with the § 102(b) rejection based on Rees et al., Applicants request that the Examiner specifically identify the relied upon sync signal that is purportedly used to synchronize the clock.

The Examiner's rejection is even more deficient with respect to the dependent claims. For example, dependent claims 41 and 43 recite that the "the time stamp clock of each of the plurality of event collection cards are synchronized together," and claims 42 and 44 recite a "clock source for sending the sync signal to each of the plurality of event collection cards." For each of these claims, the Examiner cites to the same portion of Rees et al. describing how probe 20 synchronizes the received tags to the probe's internal clock. Nothing, however, in this cited section of Rees et al., or any other section of Rees et al., describes synchronizing together the time stamp clocks of respective probes 120, or describes that multiple probes 120 receive a common sync signal from a common clock source. In particular, Rees et al. does not disclose at least that the "the time stamp clock of each of the plurality of event collection cards are synchronized together," as recited in claims 41 and 43, or a "clock source for sending the sync signal to each of the plurality of event collection cards," as recited in claims 42 and 44. Thus, these claims are allowable over Rees et al. for these additional reasons.

The Examiner also rejected claims 6-9 under 35 U.S.C. § 103 as unpatentable over Rees et al. and Nouri (U.S. Patent No. 6,073,255). The Examiner relies upon Nouri for its apparent disclosure of a master card synchronizing to a slave card. Since Nouri fails to cure the above deficiencies of Rees et al., and since claims 6-9 ultimately depend from claim 1, these claims are allowable for the reasons given above.

The Examiner also rejected claims 10, 11, 36, and 37 under 35 U.S.C. § 103 as unpatentable over Rees et al. and Hershey (U.S. Patent No. 5,375,070). The Examiner relies upon Hershey for its apparent disclosure of a bus isolation unit. Since Hershey also fails to cure the above deficiencies of Rees et al., however, and since claims 10, 11, 36, and 37 depend from claims 1 or 28, these claims are similarly allowable for the reasons given above.

Accordingly, claims 1 and 28 are thus allowable over Rees et al., as well as any possible combination of Rees et al. with Nouri and/or Hershey. Because claims 2-15 and 29-44 ultimately depend from either claim 1 or 28, these claims are allowable for at least the reasons given above for claims 1 and 28.

Therefore, in view of the foregoing remarks, Applicants respectfully request the reconsideration and reexamination of this application and the timely allowance of pending claims 1-15 and 28-44.

Applicant believes no fee is due with this response other than as indicated on the enclosed fee transmittal. However, if a fee is due, please charge our Deposit Account No. 18-1945, under Order No. BBNT-P01-001 from which the undersigned is authorized to draw.

Dated: June 10, 2004

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